BCA
Second Semester
Digital Logic & Design
(BCA- 06)

Duration: 3Hrs. **Full Marks: 70**

Part-A (Objective) =20
Part-B (Descriptive) =50

PART-B (Descriptive)

Duration: 2 hrs. 40 mins. **Marks: 50**

I. Answer the following questions (any five) **2 x 5=10**

a) Divide $(101101)_2$ by $(110)_2$

b) Prove that AB+A(B+C)+B(B+C)=B+AC

c) What is the octal equivalent of hexadecimal number(B9F.AE)

d) Simplify the given Boolean expression

Y=A+$\bar{A}$B+$\bar{A}\bar{B}$C+$\bar{A}\bar{B}\bar{C}$D

e) Draw the circuit diagram of full subtractor.

f) Explain the difference between a sequential circuit and combinational circuit.

g) Give the characteristic table and excitation table of JK flip flop.

Answer the following questions (any five) **5X3=15**

a) Minimize the following function

$$AB + A\bar{B}C\ (\bar{B}\ \bar{C}+C) + \overline{AC}$$

b) Given the logic function of three variables

f(A,B,C)=A+$\bar{B}$C. Express f in the standard SOP form.

c) Design 1X4 demultiplexer.

d) Minimize the following function using K-map.

$F(A,B,C,D)=\sum m(1,3,7,11,15)+\sum d(0,2,5)$

e) Design 4X16 decoder using 3X8 decoder.

f) Construct T flip flop using SR flip flop.

g) Design a 2X4 decoder with enable inputs.

III. Answer the following questions (any five) **5X5=25**

a) Convert $(1011)_2$ and $(101)_2$ into decimal numbers. Multiply them and then convert the result into binary.

b) Realize following function using 8:1 multiplexer.

$Y(A,B,C,D)=ABC+ABD+AB\bar{C}\bar{D}+\bar{A}B\bar{C}D$

c) Implement a full adder with two half adders and an OR gate.

d) Design a counter which counts decimal values

0, 1, 3,4,5,6

e) Give the state diagram of SR flip flop.

f) Implement the following function using 8:1 MUX.

$F(A,B,C,D)=\sum(0,1,3,6,8,9,14,15)$

g) Write short notes on any one of the following

a) Multiplexer

b) Shift Register

c) MOD-6 synchronous counter.

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BACHELOR OF COMPUTER APPLICATION

Second Semester

Digital Logic & Design

(BCA- 06)

(The figures in the margin indicate full marks for the questions)

Duration: 20 minutes **Marks – 20**

(PART A- Objective)

Time: 20 mins **Total Marks: 20**

I. Choose the correct answer from the following: **1×20=20**

1. Radix of binary number system is___?
   a) 0 b) 1
   c) 2 d) A &B

2. A group of four bits is known as
   a) Bit b) Byte
   c) Nibble d) Word

3. 1's complement representation of decimal number of -17 by using 8 bit representation is
   a) 11101110 b) 11011101
   c) 11001100 d) 00010001

4. The Gray code for decimal number 6 is equivalent to
   a) 1100 b) 1001
   c) 0101 d) 0110

5. The binary equivalent of octal number (367.52) is
   a) 010101111.101010 b) 011110111.101010
   c) 111100111.101010 d) 111110111.101010

6. The hexadecimal number 'A0' has the decimal value equivalent to

a) 80 b) 256
c) 100 d) 160

7. The NAND gate output will be low if the two inputs are

a) 00 b) 01
c) 10 d) 11

8. DeMorgan's first theorem shows the equivalence of
a) OR gate and Exclusive OR gate
b) NOR gate and Bubbled AND gate
c) NOR gate and NAND gate
d) NAND gate and NOT gate

9. If X, Y and Z are Boolean variables, then the expression $X(X+\bar{X}Y)$ Z(X+Y+Z) is equal to

a) $X+\bar{X}Y$ b) X+Y+Z
c) XYZ d) XZ

10. The simplified form of a logic function $Y=AB+\bar{A}+\bar{B}$ is

a) AB b) $\bar{A}+\bar{B}$
c) 1 d) 0

11. How many two –input AND and OR gates are required to realize Y=CD+EF+G

a) 2, 2 b) 2, 3
c) 3, 3 d) None of these

12. Which of the following is a universal gate?

a) AND b) NAND
c) OR d) NOT

13. A full adder logic circuit will have
a) Two inputs and one output

b) Three inputs and three outputs
c) Two inputs and two outputs
d) Three inputs and two outputs

14. The gates required to build a half adder are
a) Ex-OR gate and NOR gate
b) Ex-OR gate and OR gate
c) Ex-OR gate and AND gate
d) Four NAND gates

15. How many select lines will a 16 to 1 multiplexer will have
a) 4
b) 3
c) 5
d) 1

16. One example of combinational circuit is
a) Adder
b) Counter
c) Shift register
d) Flip-flop

17. A demultiplexer has _____
a) One data input, a number of selection inputs and they have several outputs
b) One output and one input
c) Several inputs and several outputs.
d) Several inputs and one output

18. How many flip- flops are required for Mod-16 counter?
a) 5
b) 6
c) 3
d) 4

19. In a JK flip-flop, toggle means
a) Set Q=1 and $\bar{Q}$=0
b) Set Q=0 and $\bar{Q}$ =1
c) Change the output to the opposite state
d) No change in output.

20. A ring counter consisting of five flip-flops will have
a) 5 states
b) 10 states
c) 32 states
d) infinite state.

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